

Declaration of Thomas Wiegand

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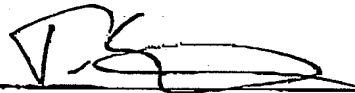
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DECLARATION OF THOMAS WIEGAND UNDER 37 CFR § 1.131

1. My name is Thomas Wiegand and I am an inventor of the invention claimed in the above referenced patent application.
2. The Examiner has rejected Claims 1-5, 10-16, and 21-26 of my patent application under 35 U.S.C. 102 (a) as being anticipated by the document "Proposed Clean Up Changes for Cabac." I am also an author of this document.
3. The Information Disclosure Statement which was submitted with this application listed this document as having a publication date of October 2002. In fact, the actual publication date of this document is 9 October 2002. I attach hereto a copy of the document supporting this publication date as Exhibit A.

4. Further, the cited reference itself is not prior art for the reason that it comprises a publication by myself, and my co-inventor, and one other individual. Thus, to the extent that the cited reference teaches my invention, the teaching is my own teaching and not that of another.

6. All statements made of my own knowledge are true, and all statements made on information and belief are believed to be true. I understand that willful false statements and the like are punishable by fine or imprisonment or both (18 U.S.C. § 1001) and may jeopardize the validity of this application or any patent issuing thereon.



Thomas Wiegand

16.4.02
Date

Exhibit A

Title: Proposed Cleanup Changes for CABAC

Status: Input Document to JVT

Purpose: Proposal

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1 Summary

In this document, we propose a couple of cleanup changes to the specification of the CABAC entropy coding part in the current draft [1]. Although the proposed changes are very minor in terms of changes to the draft text, the resulting improvements with respect to complexity and coding efficiency are quite significant.

2 Proposed Technical Changes

2.1 Coding of Intra Prediction Modes for 4x4 Luma Blocks

In the current draft, coding of Intra 4x4 and SI Intra 4x4 prediction modes for a given block uses 18 different context models depending on the prediction mode chosen for the neighboring 4x4 block to the left. In JVT-D025 [2], a proposal was made to simplify context modeling in that case. More specifically, it was proposed to use only two different context models. The first model should be used to encode the binary-valued parameter `use_most_probable_mode`, which indicates the usage of the most probable mode for a given block with respect to the chosen modes of the neighboring blocks. For encoding of the parameter `remaining_mode_selector` that indicates the chosen prediction mode in the case the most probable mode is not chosen a second model is proposed to be used in conjunction with a truncated unary binarization. It was shown that these simplifications did not hurt the coding efficiency for the common test set [2].

We re-examined the proposed simplifications of JVT-D025 and found that a further modification is useful. In contrast to JVT-D025 we have chosen a fixed-length binarization with a length of 3 bits to encode the `remaining_mode_selector`. Since for the non-CABAC case, a 3 bit fixed-length codeword is transmitted for the `remaining_mode_selector`, a better harmonization with the CAVLC/UVLC entropy coding mode is achieved.

To evaluate the performance of our proposed simplification in conjunction with JVT-D025, a set of experiments has been conducted using JM 4.0d as a common basis. The results of these simulations for the common test set and the interlaced test set are summarized in Tables 1 and 2, respectively. It turned out that in comparison to the method currently specified in the FCD an average bit rate reduction of approximately 0.4% could be achieved in all observed cases.

Table 1: Average Bjontegaard Delta bit rate savings in % for the QP-range = 28, 32, 36, 40 for the common test set (QCIF/CIF) using the first intra frame only for a performance comparison of the proposed changes to the FCD (positive values reflect a bit rate reduction).

Container	Foreman	News	Silent	Paris	Tempete	Mobile	Average
0.11	0.47	0.24	0.73	0.42	0.65	0.26	0.41

Table 2: Average Bjontegaard Delta bit rate savings in % for the QP-range = 28, 32, 36, 40 for the interlaced test set using the first intra frame only for a performance comparison of the proposed changes to the FCD (positive values reflect a bit rate reduction).

Usage of ABT	Canoe	F1	Rugby	Mobile	Football	Average
No	0.82	0.20	0.27	0.12	0.45	0.37
Yes	0.58	0.40	0.40	0.20	0.51	0.42

2.2 Simplified Coding of Intra Prediction Modes for Chroma Blocks

A rather minor change is proposed to simplify coding of intra prediction modes related to chroma blocks. Here we propose to reduce the number of different context models from 5 to 4. To be more specific, we propose to set $\text{max_idx_ctx_id} = 2$ instead of $\text{max_idx_ctx_id} = 3$, as specified in the current draft. By doing so, no negative impact on coding efficiency has been observed.

2.3 Changes for MB-Adaptive Frame/Field Coding

For a frame picture in MB-level adaptive coding of interlaced sources, the selection of frame or field coding is done at MB level. Thus, a binary-valued frame/field flag `mb_field_decoding_flag` is required to indicate if the 2 MBs of a MB pair shall be decoded in frame or field mode.

For coding of `mb_field_decoding_flag`, we propose the following context model. Let A and B denote the spatially neighboring MB pairs to the left and on top of the current MB pair X, respectively, then we choose the conditioning term `ctx_mb_field(X)` according to the template `ctx_var_spat1` as specified in [1]:

$$\text{ctx_mb_field}(X) = ((\text{mb_field_decoding_flag}(A) \neq 0) ? 1 : 0) + ((\text{mb_field_decoding_flag}(B) \neq 0) ? 1 : 0)$$

This results in 3 additional context models for coding of `mb_field_decoding_flag`.

Coding of all other syntax elements is done in exactly the same way as specified in the FCD [1]. Only the semantics of a neighboring macroblock used for conditional coding of the `mb_skip_flag` has to be specified more precisely for the case of MB-adaptive frame/field coding. Since the decoder may not know the specific choice of frame or field mode when decoding the `mb_skip_flag`, it is always assumed that co-location of macroblocks for context determination has to be interpreted as co-location in the sense of pure frame coding. That means, for instance, that the macroblock B on top of the current skipped macroblock X in a (potential) top field position is always chosen as the bottom field MB of the MB pair above the current MB X.

2.4 Changes for Improving the Arithmetic Coding Engine

2.4.1 Modified Renormalization Bound and Initialization of Range

In the current FCD [1], renormalization in the arithmetic coding engine is performed such that the range R of the coding interval stays within $[Q+1, Q+2, \dots, 2*Q]$, where $Q = 0x4000$. This convention has the drawback that the underlying renormalization condition $R \leq Q$, which has to be tested each time the range R has been modified, cannot be implemented by using simple bit

operations. In addition, for specifying the LPS related sub-interval range R_{LPS} from the given range R , a further subtraction is needed: $R_{LPS} = \text{RTAB}[\text{state}][(\text{R}-0\text{x4001})\gg 12]$.

To avoid these operations, we propose to modify the renormalization bound such that $R \in [Q, Q+1 \dots, 2*Q-1]$. This implies that the comparison for renormalization is exchanged by the test of the condition $R < Q$ (which can be realized by a simple bit test), and that the computation of the LPS related range R_{LPS} is now given by $R_{LPS} = \text{RTAB}[\text{state}][(\text{R}\gg 12) \& 0\text{x03}]$. At the same time, however, we have to change the initial value of R from $2*Q$, as currently specified in the draft, to the value of $2*Q-2$. The reason behind not choosing $2*Q-1$ as the initial value is given by the fact that for a proper equi-sized sub-interval partitioning in the case of a decoder bypass for uniform pdfs (as specified in subclause 9.2.4.2.5 of [1]) we have to maintain an even-valued range.

2.4.2 Simplified Decoder Bypass

As currently specified in the draft, the minimum precision for representing the range and value register at the decoder is given by 16 bits. In fact, as part of this proposal (see section 2.4.3) we will show that this precision can be further reduced by means of a simple change in the initialization part of the coding engine.

Under the assumption that one bit more of precision than the minimum number of bits is available for representing the R (range) register and V (value) register at the decoder, a further simplification for the decoder bypass is possible. Instead of computing $R_{half} = R/2$ in the first step as specified in subclause 9.2.4.2.5 of [1], we propose to first double the value register V , i.e., $V \leftarrow V \ll 1$. This way the computation of $R_{half} = R/2$ can be omitted, and each of the subsequent steps involving R_{half} can be replaced by the corresponding operation in which R_{half} is replaced by R , as depicted in Figure 1.

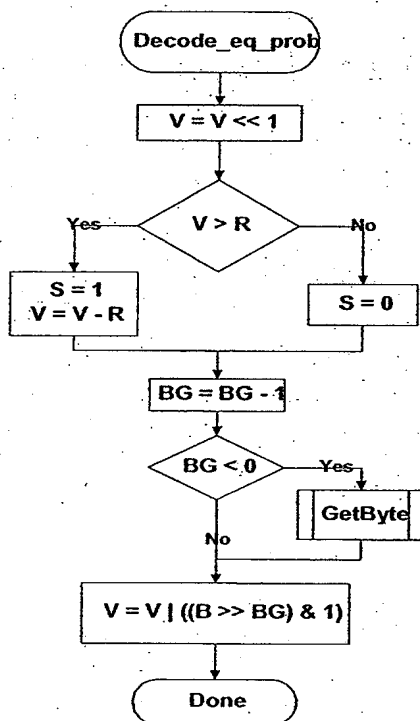


Figure 1: Flowchart of simplified decoder bypass

2.4.3 12-bit Implementation of the Coding Engine

As specified in subclause 9.2.4.2.2 of the current draft [1], the LPS related range values R_{LPS} are actually given in 8-bit precision. For a convenient access in a 16-bit architecture, however, the corresponding table entries of RTAB are given as multiples of 64. Thus, under the condition that the range R has to be represented by an even value, there are 5 LSB bits that are unused in a 16-bit implementation. By further changing the initial value of R from the value of $2 \cdot Q - 2$ as proposed in section 2.4.1 to the value of $2 \cdot Q - 2 \cdot 32$, we finally arrive at a minimum precision of 11 bits both for the R and the V register by simply downshifting (right shifting) the 5 unused LSB bits. By taking into account the additional bit of precision required for the simplified decoder bypass (see section 2.4.2), we finally arrive at a minimum number of 12 bits of precision for the registers R and V representing the arithmetic decoding engine.

2.4.4 Speedup of Renormalization (non-normative)

In case of having available a higher precision for representing R and V , for example, in a software-based implementation with a 32-bit integer representation, the following trick can be used to speed up the renormalization loop.

According to the specification given in [1], a bit is inserted in the least significant bit of V each time a renormalization shift occurs, as is shown in the last block of the flowchart in Fig. 1. By left shifting V , R , all RTAB entries, all related bounds and initial values as well by 7 bits, i.e., by multiplying these registers by 2^7 , which requires a minimum register precision of 19 bits according to the changes proposed in the previous section, a full byte can be inserted in the 8 least significant bits of the V register for each call of the GetByte procedure. In fact, by using an even higher precision of 27 bits, which corresponds to a left shift of 15 bits, the byte-wise insertion can be further replaced by a word-wise insertion. This way the renormalization loop is reduced to essentially three simple operations, which can be done in parallel: two shift operations (for the registers R and V) and one counter decrement.

3 Verification of JVT-D019 (Constrained Arithmetic Coding)

In this section we provide some experimental results for verification of the constrained arithmetic coding as presented in JVT-D019 [3]. For the previously specified constrained arithmetic coding in the CD [4], a quite significant loss in coding efficiency of up to 7% overall bit rate increase was reported [3]. We re-examined the new constrained arithmetic coding algorithm with respect to the specific low bit-rate coding scenarios investigated in [3]. For this experiment we used the test model, version JM4.0d, which already includes the constrained arithmetic coding as proposed in JVT-D019. We compared two variants of the encoder: the original version using the method of constrained coding (triggered by switching the pre-processor flag `NEW_CONSTRAINT_AC` on), and the second version, where the constrained arithmetic coding has been disabled (by commenting out the pre-processor flag `NEW_CONSTRAINT_AC`). The results of these experiments, which can be found in the accompanying Excel-file [JVT-E059.xls](#), clearly show that there is no difference in coding efficiency between these both versions for the observed cases.

References

- [1] Th. Wiegand, Editor's Proposed Draft Text Modifications for Joint Video Specification (ITU-T Rec. H.264 | ISO/IEC 14496-10 AVC), Draft 7, JVT-E022d7, Sept 2002.
- [2] M. Karczewicz, Analysis and Simplification of Intra Prediction, JVT-D025, July 2002.
- [3] D. Marpe et al., Proposed Editorial Changes and Cleanup of CABAC, JVT-D019, July 2002.
- [4] Th. Wiegand, Joint Committee Draft (CD), JVT-C167, May 2002.

(Append for Proposal Documents)

JVT Patent Disclosure Form

International Telecommunication Union
Telecommunication Standardization Sector



International Organization for Standardization



International Electrotechnical Commission



Joint Video Coding Experts Group - Patent Disclosure Form

(Typically one per contribution and one per Standard | Recommendation)

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Geneva, CH, 9-17 October, 2002

Relevant Recommendation | Standard and, if applicable, Contribution:

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Title

Proposed Cleanup Changes for CABAC

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